ECE

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 31210

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2012.

Third Semester

Electronics and Communication Engineering

EC 1201 — DIGITAL ELECTRONICS

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Convert 41.6875_{10} to binary.
2. Construct AND gate using NAND gates.
3. Define the term fan-out.
4. Define propagation delay.
5. Give the circuit and truth table of Half–adder.
6. Define Multiplexer.
7. Draw the logic diagram of D flipflop using NAND gates.
8. Give the excitation table for JK flipflop.
9. Differentiate ROM and RAM.
10. Briefly differentiate PLA and PAL.

PART B — ($5 \times 16 = 80$ marks)

11. (a) Minimize the functions using suitable Boolean laws

(i) $A + \overline{B}C\left(A + \overline{\overline{B}C}\right)$ (5)

(ii) $A\left[B + C\left(\overline{AB + AC}\right)\right]$ (5)

(iii) $\left[\overline{A\overline{B} + ABC} + A\left(B + A\overline{B}\right)\right]'$. (6)

Or

(b) Reduce the function F in sum of products and products of sum

$F = \sum m(0,1,2,3,7,8,10)$

$d = \sum m(5,6,11,15)$

where 'd' represents dont cares. (16)

12. (a) Explain the construction and operation of DTL and TTL NAND gate. Also mention the characteristics of DTL and TTL families. (16)

Or

(b) (i) Explain CMOS NAND and NOR gate operation. (8)

(ii) Detail the working of tristate logic. (8)

13. (a) (i) Design and implement 8×1 multiplexer using suitable gates. (8)

(ii) Design 3 bit parity generator and checker circuit. (8)

Or

(b) (i) Design and implement full subtractor using suitable gates. (8)

(ii) Design the logic diagram of Magnitude comparator to compare two binary variables A and B accompanied by 3 bits each. (8)

14. (a) (i) Give the logic diagram, truth table and excitation table for JK flipflop. (8)

(ii) Design a 2 bit asynchronous down counter. (8)

Or

(b) (i) Design a decade synchronous up counter using 'T' flipflops. (8)

(ii) Explain 3 bit parallel in serial out shift register. (8)

15. (a) Write a note on :

(i) EEPROM (4)

(ii) Static RAM Cell (4)

(iii) Dynamic RAM Cell (4)

(iv) Bipolar RAM Cell. (4)

Or

(b) (i) Implement the boolean functions F_1 and F_2 with a PLA

$$F_1(A,B,C) = \sum m(0, 1, 2, 4)$$

$$F_2(A,B,C) = \sum m(0, 5, 6, 7).$$ (8)

(ii) Design a combination circuit using ROM for a circuit that accepts a 3 bit number and generates an output binary equal to the square of the input number. (8)